FPGA is a versatile and low cost prototyping board which helps to decrease the time to market by providing a platform to specify, design and analyze a proposed architecture without developing the actual silicon chip. FPGA is an ideal platform for specifying, modeling and verifying the logic design of protocol processors used for data processing in the network layer, which ultimately reduces the flaws in the end product.

The main objective of this thesis is to speed up the process of prototyping protocol processor architectures on FPGA. To achieve this objective, the goal was to define a design process that would enable rapid FPGA prototyping. To test the suggested process the internet checksum calculation of the IP protocol has been designed and implemented on FPGA. Xilinx Platform Studio has been used to design software and hardware specification flows for embedded protocol processor design. The work has been targeted to the Xilinx ML310 FPGA platform.

Based on the presented experiment, it was observed that the suggested design process was suitable for rapid hardware prototyping of protocol processing functions.

**Keywords**
Prototyping, FPGA, ML310 Platform, Network layer, Internet Checksum, IPv6, Protocol Processor Prototyping.