In the thesis a development method based on high level modeling and automated VHDL code generation is studied. The functionality and suitability of the method for the development and further implementation of a signal processing algorithm on a FPGA is evaluated.

The principles of traditional development methods are presented on general level, and the differences between those and the method used in this thesis are discussed. The basic principles of model-based design methodology are shortly introduced.

Two-dimensional discrete cosine transform is used as an example algorithm. The mathematical foundation of the algorithm is presented, together with the presentation of the structure of the fast discrete cosine transform implemented in this thesis. Several alternative approaches for implementation are discussed.

The algorithm is implemented in MATLAB / Simulink environment using Xilinx System Generator for DSP to create the fixed point simulation model and the VHDL source code. The model is simulated throughout the implementation phase on high abstraction level with both floating point and fixed point precision. The generated VHDL description is synthesized for Virtex-II FPGA using Xilinx ISE development suite. The functionality of the design is verified on register transfer level by using ModelSim simulator.

Finally it is evaluated how the model-based development method implemented algorithm performs when compared to existing commercial solutions, and how this particular method meets the expectations to increase the efficiency of the development work.

A general impression is that the development method is mature, increases the efficiency of the development work and produces results which perform well in comparison to commercial solutions. During this research work, a novel idea for implementing a matrix transposition was invented and a related patent is pending in United States.

Keywords:
FPGA, discrete cosine transform, VHDL, Xilinx, MATLAB, Simulink